Society for Promotion of Excellence in Electronics Discipline

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SPEED e- NEWSLETTER

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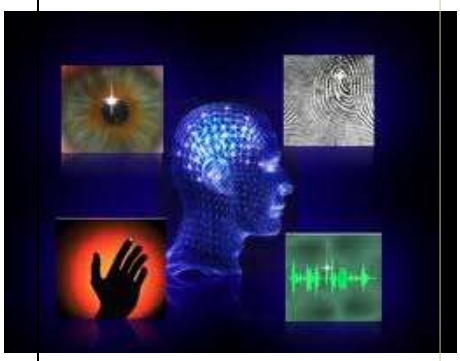
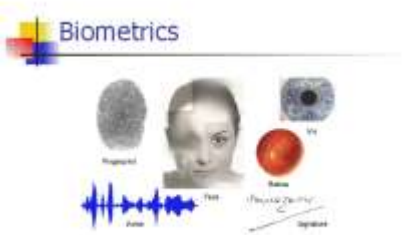


Biometrics

Main Article

Humans recognize each other according to their various characteristics for ages. We recognize others by their face when we meet them and by their voice as we speak to them. Identity verification (authentication) in computer systems has been traditionally based on something that *one has* (key, magnetic or chip card) or *one knows* (PIN, password). Things like keys or cards, however, tend to get stolen or lost and passwords are often forgotten or disclosed.

To achieve more reliable verification or identification we should use something that really characterizes the given person. Biometrics offer automated methods of identity verification or identification on the principle of measurable physiological or behavioural characteristics such as a fingerprint or a voice sample. The characteristics are measurable and unique. These characteristics should not be duplicable, but it is unfortunately often possible to *biometrics* create a copy that is accepted by the biometric system as a true sample.

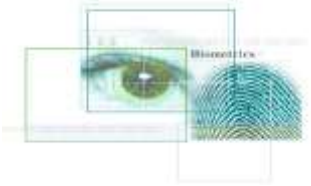


Biometrics (or **biometric authentication**) is a branch which deals with the identification of humans by their characteristics. Biometrics is used as a form of identification and access control. It is also used to identify individuals in groups that are under surveillance.

Biometric systems can be used in two different modes. Identity *verification* occurs when the user claims to be already enrolled in the system (presents an ID card or login name); in this case the biometric data obtained from the user is compared to the user's data already stored in the database. *Identification* (also called *search*) occurs when the identity of the user is a priori unknown. In this case the user's biometric data is matched against all the records in the database as the user can be anywhere in the database or he/she actually does not have to be there at all.

Figure 1

It is evident that identification is technically more challenging and costly. Identification accuracy generally decreases as the size of the database grows. For this reason records in large databases are categorized according to a sufficiently discriminating characteristic in the biometric data. Subsequent searches for a particular record *identification* are searched within a small subset only. This lowers the number of relevant records per search and increases the accuracy (if the discriminating characteristic was properly chosen). Before the user can be successfully verified or identified by the system, he/she must be registered with the biometric system. User's biometric data is captured, processed and stored. As the quality of this stored biometric data is crucial for further authentications, there are often several (usually 3 or 5) biometric samples used to create user's master template. The process of the user's registration with the biometric system is called *enrollment*.



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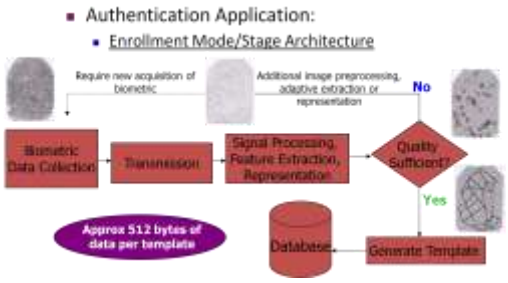
Biometrics…….

"*We love those subjects which we understand and later work on it.*"
-N. M. Kulkarni

Most significant difference between biometric and traditional technologies lies in the answer of the biometric system to an authentication/ identification request. Biometric systems do not give simple yes/no answers. While the password either is 'abcd' or not and the card PIN 1234 either is valid or not, no biometric system can verify the identity or identify a person absolutely. The person's signature never is absolutely identical and the position of the finger on the fingerprint reader will vary as well. Instead, we are told how similar the current biometric data is to the record stored in the database. Thus the biometric system actually says what is the Biometric Systems probability that these two biometric samples come from the same person.

Biometric technologies can be divided into 2 major categories according to what they measure:
* Devices based on physiological characteristics of a person (such as the fingerprint or hand geometry).
* Systems based on behavioral characteristics of a person (such as signature dynamics).

Biometric systems from the first category are usually more reliable and accurate as the physiological characteristics are easier to repeat and often are not affected by current (mental) conditions such as stress or illness.



One could build a system that requires a 100% match each time. Yet such a system would be practically useless, as only very few users (if any) could use it. Most of the users would be rejected all the time, because the measurement results never are the same. We have to allow for some variability of the biometric data in order not to reject too many authorized users. However, the greater variability we allow the greater is the probability that an impostor with a similar biometric data will be accepted as an authorized user. The variability is usually called a (security) threshold or a (security) level. If the variability allowed is small then the security threshold or the security level is called *high* and if we allow for greater variability then the security threshold or the security level is called *low*.

Applications

The most common biometric system application used today is AFIS, the automatic fingerprint identification systems, used in forensics for the identification of convicted criminals. Recent advancements in biometric sensors and matching algorithms have resulted in widespread employment of biometrics in numerous civilian and government establishments. Specific applications include terminal and network access, sign-on (log-on) restrictions, data protection, wireless and remote access limitations, transaction security, and Web security

Dr. N. M. Kulkarni

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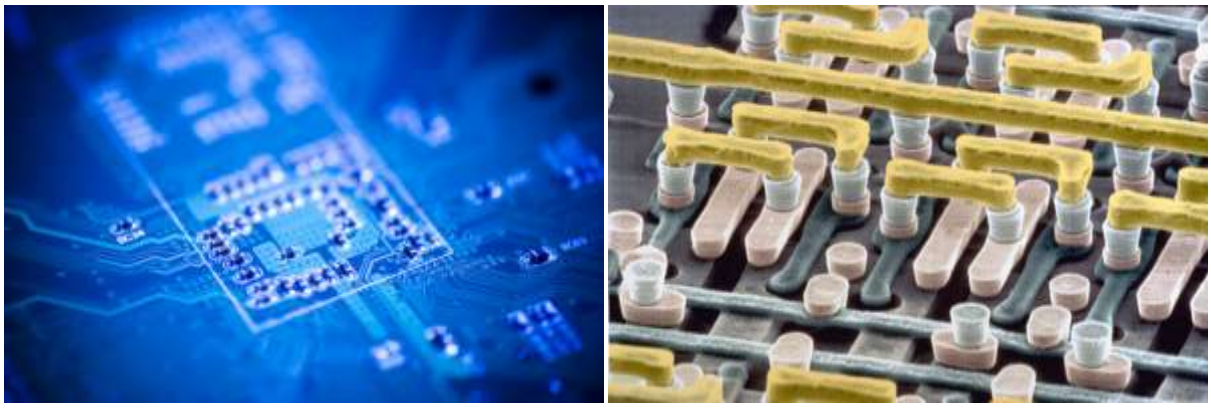
Specialized Human Resource Development need in the domain of IC Layout Design

In recent years, electronics the world over has made unprecedented growth in terms of new technologies, new ideas and principles. The rate of obsolescence of technologies also has been extremely high. Researchers, academicians, industries and the society at large have to work in unison to meet the challenges of the rapidly growing discipline.



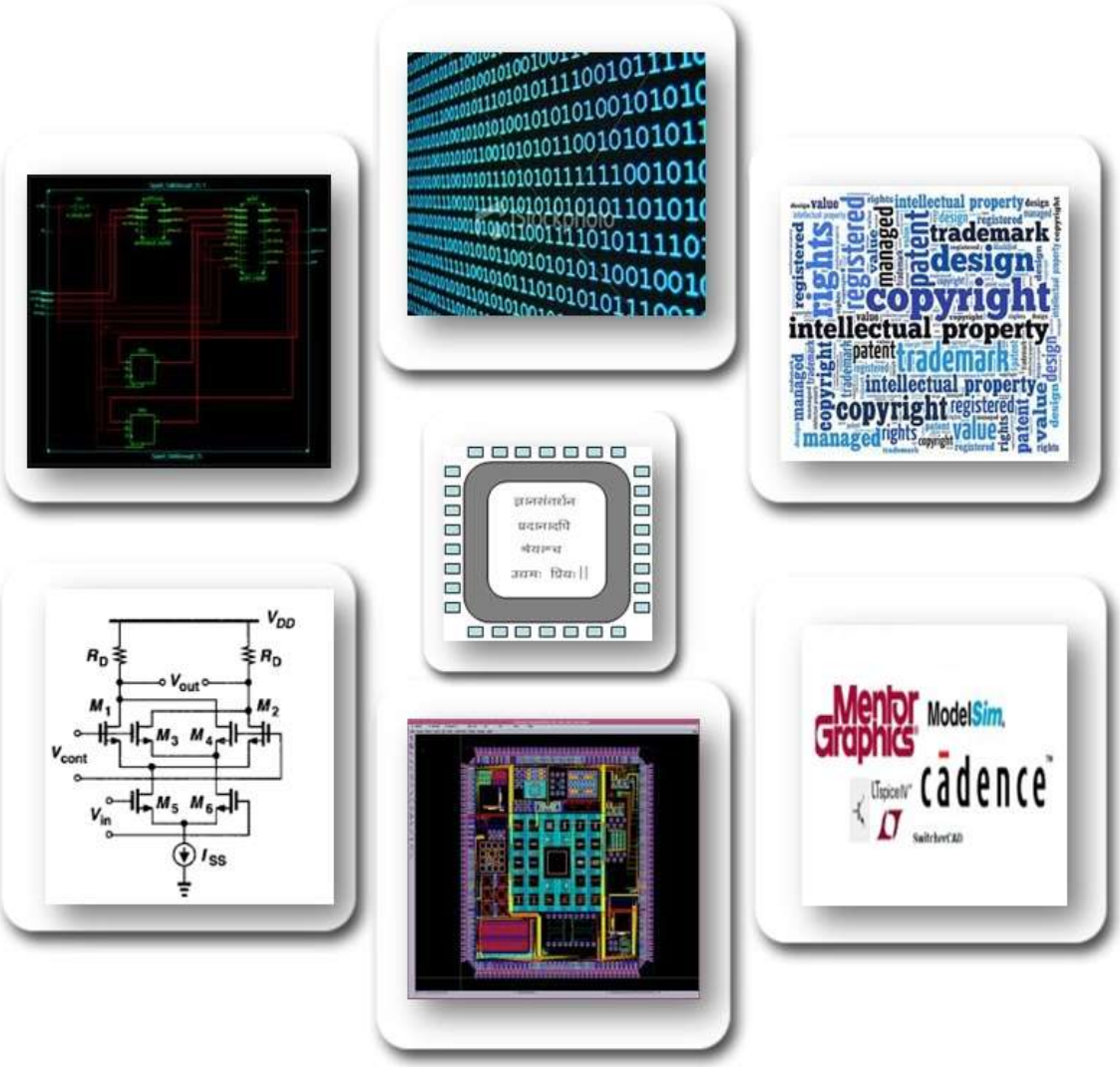
The research organizations and industries that work in this frontier area are in need of highly skilled and scientifically oriented manpower. The IC layout design over the years has become main source of IP (Intellectual Property) for the company with the trends in re-use of the earlier created works and also the ever increasing complexities of the systems leaving little room for fresh development works costing millions of dollars and huge time.

The importance of protection of created chip IPs has thus become a most sought global protection to enable IC designer protect their original woks from unauthorized use. In the country, with the Government initiative of establishing SICLDR (Semiconductor Integrated Circuit Layout Design Registry) to give IP protection to works generated, it also becomes imperative to generate the specialized type of human resource well versed with the IP matters and technical expertise in Layout design fields to support national efforts in Semiconductor IP protection. Presently, t*here is acute shortage of skilled human resource in the country in the IC layout Design and IP fields which needs to be addressed.*

A survey of major educational institutions offering courses related to VLSI design indicate these to be dominantly on the IC design mythologies and design approaches. None of these have courses in totality of IC Layout Design from conception, creation of IP, creation and evaluation of the chip Layout Designs and likely infringement issues etc as core subjects. Hence there is a dire need for a evolving a dedicated UG/PG program which offers technical exposure in IP matters and Layout Design fields.

Department of Electronic Science, University of Pune, initiating a New PG Diploma course in IC Layout design, aimed to give an interested exposure to both IC design and IP areas; and generate specialized human resource trained in these aspects to feed R&D institutes and industry. The new PG Diploma course would cover the details of CMOS Design, Analog as well as Digital Design, IC Layout Design with hands on practice on industry standard design tools from Cadence and Mentor Graphics. Aspects related to the Intellectual Property (IP) generation and management will also form a major part of the course. The 10 month duration PG Diploma Course is proposed to be conducted at the

Department of Electronic Science, University of Pune, starting from 3rd December 2012. A national level Entrance examination for admission to the course is scheduled on 24th November 2012. More details are available in the separate advertisement and on the department website https://electronics.unipune.ac.in



UNIVERSITY OF PUNE
DEPARTMENT OF ELECTRONIC SCIENCE
ADMISSION NOTIFICATION
POST GRADUATE DIPLOMA IN
IC LAYOUT DESIGN

Last date of Application: 22nd November2012
Date of Entrance Exam: 24th November 2012
Course start on : 3rd December 2012
For details visit http://electronics.unipune.ac.in/
contact Head of Dept. on :+91-20-25699841,
+91-20-25691256.

Advt. No
Date :

Dr. (Capt.) C. M. Chitale
Registrar

UNIVERSITY OF PUNE
DEPARTMENT OF ELECTRONIC SCIENCE
ADMISSION NOTIFICATION

Post Graduate Diploma in "IC LAYOUT DESIGN" 2012-13

University of Pune invites application for admission to newly introduced 10 Months Post Graduate Diploma Course in IC Layout design in the Electronic Science Department. The above program is aimed to give an integrated exposure to both IC Design and IP areas; and generate specialized human resource trained in these aspects to feed R&D institutes and industry.

1. Last date of Application : 22nd November 2012
2. Date of Entrance : 24th November 2012
3. Course start on : 3rd December 2012
4. Eligibility Criteria: B.E/B.Tech in Electronics or Instrumentation, or E&TC, M.Sc. in Electronics or equivalent with at least 60% aggregate.
5. Reservation: As per Govt. of Maharashtra rules, 50%seats are reserved for SC,ST,DTNT,OBC and 3% seats are reserved for physically handicapped students.
6. No. of Seats: 40
7. Fees: Rs. 45,000/-

"Working Professionals are also invited to apply"

The details of the above addressed procedure are available on Web link: http://electronics.unipune.ac.in/ http://www.unipune.ac.in/dept/science/electronic_science/default.htm
or Head of Department on :+91-20-25699841,
:+91-20-25691256.

Advt. No
Date :

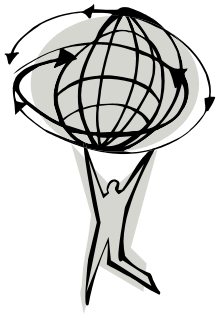
Dr. (Capt.) C. M. Chitale
Office Registrar

FORTHCOMING

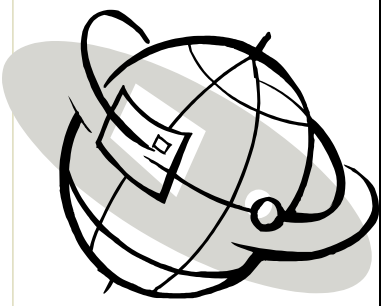
FIRST ANNIVERSARY ISSUE OF SPEED E-NEWSLETTER

All SPEED members are requested to send their CONTRIBUTIONS to mark the **First Anniversary issue of our SPEED e-Newsletter**. Students articles /contributions are also invited.

- News & Events - Photographs
- Advances in Science and Technology
- Articles related to Electronics popularization
- Cartoons
- Poems etc…



"Let us work towards Excellence in Electronics for the betterment of society"
-N. M. Kulkarni



SPEED Memberships Details

Membership Type	Fees (Rs.)
1. Patron Members	10,000
2. Life Members	2,000
3. Ordinary members	500 (per year)
4. Student	200 (per year)

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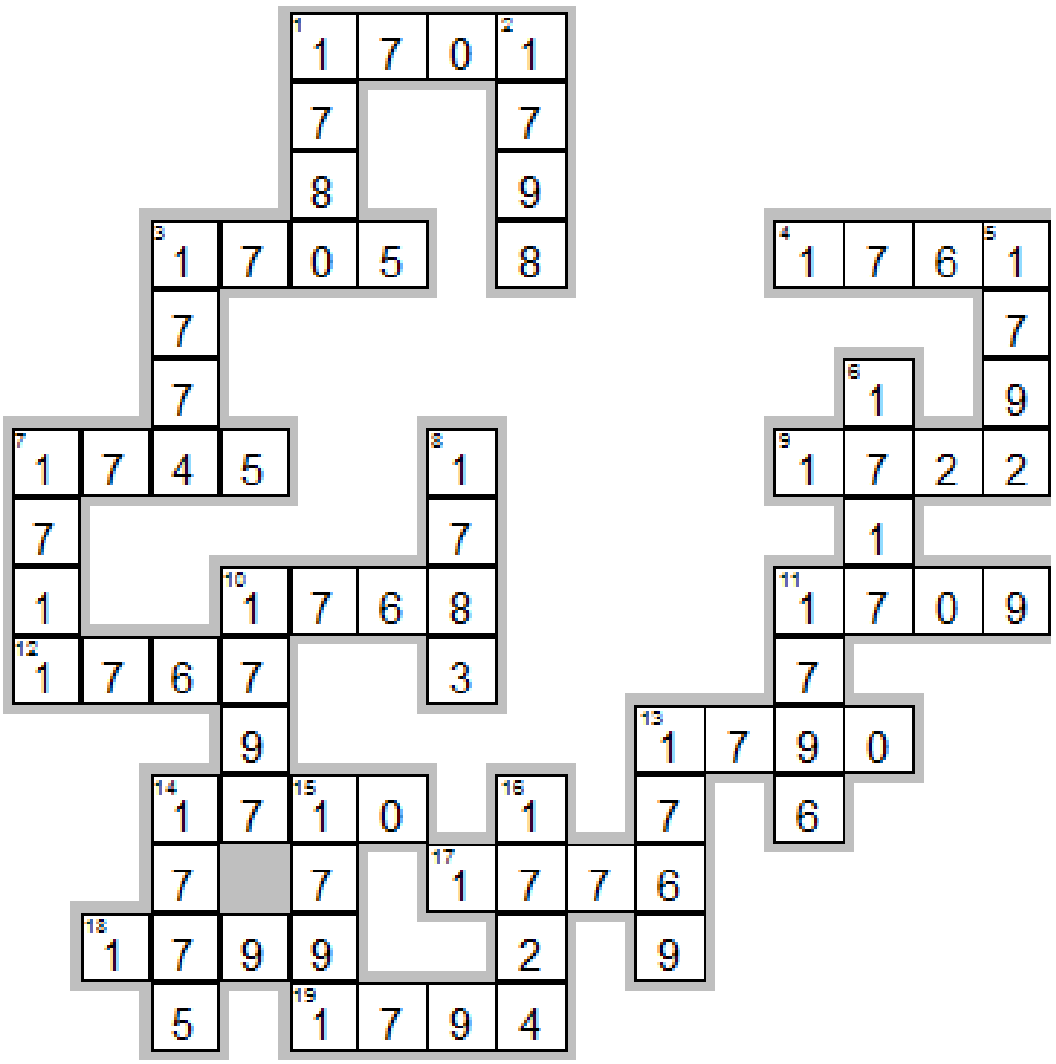
Answers of Cross-Word Puzzle of May 2012

18th Century Inventions



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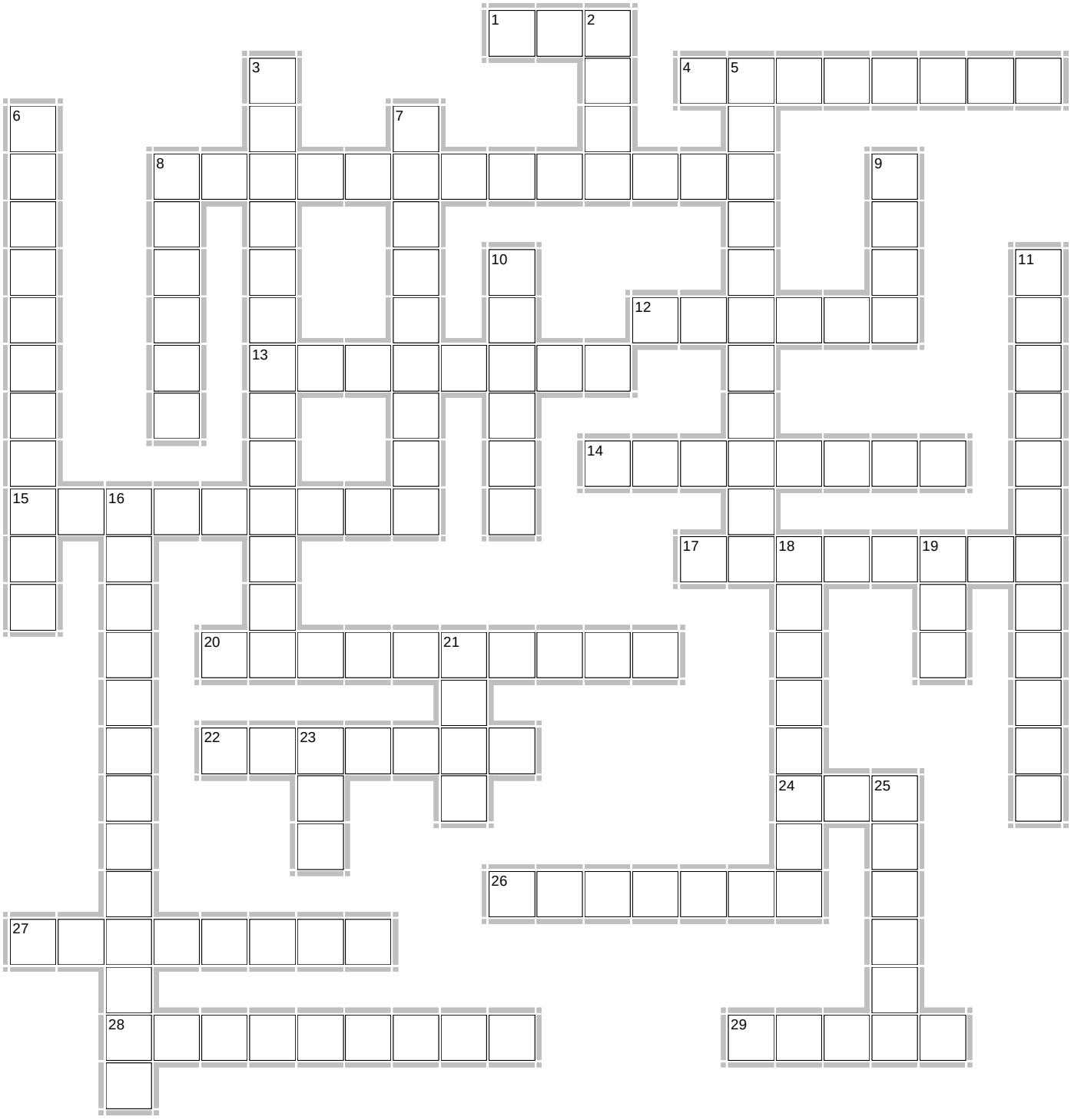
Get connected to SPEED.

We will be on the Web shortly

Student's corner: CROSS WORD PUZZLE

Crossword on Logic Families and IC specifications

Hemant Yashwant Satpute



Student's corner: CROSS WORD PUZZLE

Across

1. In TTL ICs tristate outputs are ideally suited for ___ operation. (3)
4. IN TTL ICs open collector output makes ___ operation possible. (8)
8. _____is a product of speed and power. (13)
12. In CMOS NOR gate, PMOS loads are connected in ____. (6)
13. In CMOS NOR gate, NMOS drivers are connected in ____. (8)
14. 7400 series TTL devices work ____ over a temperature range of 0 to 70 degree Celsius. (8)
15. In any logic family, when speed of operation is increased, the total amount of power dissipated in it ___. (9)
17. Two basic technologies for manufacturing digital ICs are bipolar and ____(MOS). (8)
20. Small Scale Integration refers to ____ gates on the same chip. (10)
22. 7400 series TTL devices work reliably over a ____ range of 4.75 to 5.25 volts. (7)
24. ____ is the most widely used bipolar family. (3)
26. _____ technology is preferred for SSI and MSI. (7)
27. Standard TTL has a ____ emitter input transistor. (8)
28. Standard TTL has a ____ output. (9)
29. In CMOS, fan-out may exceed ____. (5)

Down

2. Floating TTL input has the ____ effect as a high input. (4)
3. In Tristate logic when enable is equal to logic zero, then the output of the gate is in ___ state. (13)
5. Digital ICs can be classified according to the number of gates on a chip. This is referred to as level of ____. (11)
6. A group of compatible ICs with the same logic levels and supply voltages for performing various logic functions have been fabricated using a specific circuit configuration which is known as a _____. (11)
7. In TTL ICs totem pole or active pull up output ___ speed power product. (9)
8. The maximum number of TTL loads a TTL device can drive is known as the ____. (6)
9. In ____, p channel and n channel MOSFETS are connected in Series. (4)
10. In Open collector TTL NAND gate, a _____ resistor should be used. (6)
11. Using advanced ____ techniques, miniature circuits can be produced on the surface of a chip. (12)
16. ____ means the ability to connect the output of one device to the input of the other. (13)
18. The basic CMOS circuit is an _____. (8)
19. The totem pole output produces a ____ output impedance in either state. (3)
21. In Tri-state logic, third state is a ____ impedance state. (4)
23. Unipolar technology is preferred for ____ because more MOSFETs can be fabricated on the same chip area. (3)
25. CMOS has ____ speed power product and requires very small power. (6)